CLAIMS:

1. A test apparatus for testing a quiescent current of a circuit under test, the test apparatus comprising

a power supply voltage source for supplying a power supply voltage,

a switch being coupled to a terminal of the circuit under test,

a driver for controlling the switch to remove the power supply voltage from the terminal at a start of a testing cycle,

a comparator for comparing a voltage at the terminal with a reference value,

a clock generator for supplying clock pulses,

a counter for counting the clock pulses during a count period to obtain a count number, wherein the count period has a start determined by the start of the testing cycle and an end determined by an instant the voltage at the terminal crosses the reference value,

a threshold circuit for comparing the count number with a reference number to supply a pass/fail signal, and

a control circuit for controlling the value of the reference number and/or a clock frequency of the clock pulses in dependence on process parameters of the circuit under test.

2. A test apparatus as claimed in claim 1, characterized in that the circuit under test is an integrated circuit and in that the control circuit comprises an input for receiving externally determined information on a correlation between on the one hand a speed of the circuit under test and on the other hand a range of the acceptable or unacceptable values of the IDDQ for determining the value of the reference number and/or the frequency of the clock pulses based on said correlation.

3. A test apparatus as claimed in claim 1, characterized in that the device under test is an integrated circuit and in that the control circuit comprises

an oscillator for generating oscillator clock pulses having a frequency depending on the speed of the circuit under test, and

a further counter for counting the oscillator clock pulses during a predetermined period in time to obtain a further counted number determining the speed of the of the circuit under test.

4. A test apparatus as claimed in claim 2, characterized in that the externally determined information indicates an acceptable range of values of the quiescent current as function of the speed, and in that the control circuit comprises a reference number calculator with an input for receiving the externally determined information on the correlation for determining the value of the reference number being larger than an upper value of the range of values of the quiescent current at the speed relevant for the circuit under test.

5. A test apparatus as claimed in claim 3, characterized in that the control circuit comprises a reference number calculator for determining the reference number based on the correlation between the speed obtained from the further counted number and the quiescent current obtained from the counted number.

6. A test apparatus as claimed in claim 2, characterized in that the clock generator comprises a clock control circuit with an input for receiving the externally determined information on the correlation for controlling the frequency of the clock pulses supplied by the clock generator to increase when the value of the quiescent current increases.

7. A test apparatus as claimed in claim 1, characterized in that the clock generator comprises a clock control circuit for controlling the frequency of the clock pulses supplied by the clock generator based on the correlation between the speed obtained from the further counted number and the quiescent current obtained from the counted number.

8. A test apparatus as claimed in claim 1, characterized in that the threshold circuit further comprises

a difference circuit for determining a difference number being a difference between a first counted number of clock pulses during a first count period and a second counted number of clock pulses during a second count period, and

a comparator for comparing the difference number with a reference number.

9. A test apparatus as claimed in claim 8, characterized in that the difference circuit comprises a memory for storing a minimum value and a maximum value of a series of counted numbers of clock pulses respectively, the minimum value representing the first counted number and the maximum value representing the second counted number.

10. A test apparatus as claimed in claim 8, characterized in that the difference circuit comprises a memory for storing the first counted number, the second counted number being determined during the second test cycle succeeding the first test cycle.

11. A test apparatus as claimed in claim 4 or 5, characterized in that the clock generator further comprises a temperature sensor for supplying a sensed temperature of the circuit under test, and in that the reference number calculator is adapted to control the reference number based on the sensed temperature also.

12. A test apparatus as claimed in claim 6 and 7, characterized in that the clock generator comprises a temperature sensor for supplying a sensed temperature of the circuit under test, and in that the clock control circuit is adapted to control the frequency of clock pulses based on the sensed temperature also.

13. A method of testing a device under test having a terminal, the method comprises

supplying a power supply voltage via a switch being coupled to a terminal of the circuit under test,

controlling the switch to remove the power supply voltage from the terminal at a start of a testing cycle,

comparing a voltage at the terminal with a reference value,

supplying clock pulses,

counting the clock pulses during a count period to obtain a count number, wherein the count period has a start determined by the start of the testing cycle and an end determined by an instant the voltage at the terminal crosses the reference value,

comparing the count number with a reference number to supply a pass/fail signal, and

controlling the value of the reference number and/or a clock frequency of the clock pulses in dependence on process parameters of the circuit under test.

14. An integrated circuit comprising a test circuit for testing a drain to drain quiescent current drawn by at least part of the integrated circuit, the test circuit comprises

a switch being coupled to a terminal of the circuit under test,

a driver for controlling the switch to remove the power supply voltage from the terminal at a start of a testing cycle,

a comparator for comparing a voltage at the terminal with a reference value,

a clock generator for supplying clock pulses,

a counter for counting the clock pulses during a count period to obtain a count number, wherein the count period has a start determined by the start of the testing cycle and an end determined by an instant the voltage at the terminal crosses the reference value,

a threshold circuit for comparing the count number with a reference number to supply a pass/fail signal, and

a control circuit for controlling the value of the reference number and/or a clock frequency of the clock pulses in dependence on process parameters of the circuit under test.